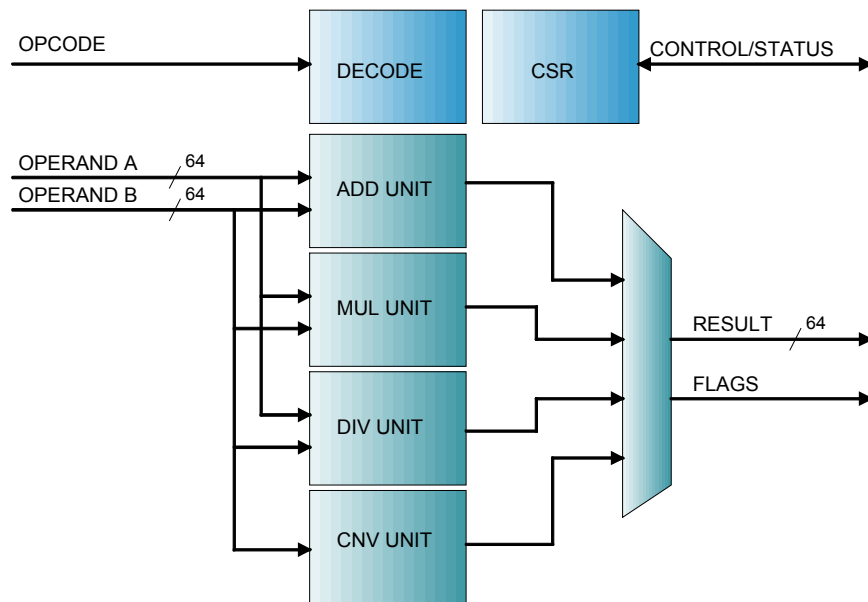


FPSD

IEEE-754 Floating Point Unit Single/Double Precision, Full Compliance



Overview

The FPSD is a co-processor unit providing floating-point computation compliant with the *ANSI/IEEE Std 754-1985, IEEE Standard for Binary Floating-Point Arithmetic* (IEEE-754 Standard). It is designed to provide high performance floating-point computation while minimizing die size and power.

The FPSD supports both single and double precision operands. The design's 3-stage execution pipeline combines high throughput with low latency, providing up to 250 MFLOPS on a 0.13u ASIC process. The host interface is clean and versatile, simplifying the interfacing to host processor pipelines.

Features

- IEEE-754 compliant
- Single and double precision instructions
- 3-stage execution pipeline
- 1-cycle throughput for most instructions
- Instructions provided
 - Add/Subtract
 - Multiply
 - Divide
 - Remainder/Modulus
 - Square root
 - Floating Point Compare
 - Double ↔ Single Format Conversions
 - Floating Point ↔ Integer Conversions
 - Round to Integer
 - Absolute Value/ Negate
 - Move
- Flag outputs support conditional branching or conditional execution
- All IEEE rounding mode supported
- All IEEE exception flags supported
- Denormals and gradual underflow supported
- Masked and unmasked exception control
- Control and status register

IEEE-754 Compliance

The FPSD is designed to provide a powerful floating-point capability that is compliant with the IEEE-754 specification. All features of the specification are implemented in the FPSD hardware design. No software support is needed to achieve compliancy.

To accommodate high performance computations, the FPSD implements two modes of operation: Full-Compliance, and Flush-to-Zero. In Full-Compliance mode, denormal numbers and gradual underflow are implemented but take extra cycles from the pipeline when they occur. In Flush-to-Zero mode, denormal numbers and underflows are flushed to zero, and the pipeline is not stalled. This feature allows the FPSD to maintain a one-cycle throughput in all operand cases when high performance is needed.

Performance

Size: 95,000 NAND Gates
 Timing: 200 MHz on 0.18u
 250 MHz on 0.13u

NOTE: The above performance data are estimates only, based on sample implementations using worst-case conditions. Achieved performance is highly dependent on the process technology, cell library, and synthesis tools used.

Instruction Timing

Instruction	Single Precision		Double Precision	
	Throughput	Latency	Throughput	Latency
Add, Subtract, Multiply, Compare, Round to Integer	1	3	1	3
Single/Double Format Conversions Integer Conversions	1	3	1	3
Absolute Value, Negate, Move	1	3	1	3
Divide	1 to 14	3 to 17	1 to 28	3 to 31
Square Root	1 to 13	3 to 16	1 to 27	3 to 30
Remainder, Modulus	1 to (e/2+2)	3 to (e/2+5)	1 to (e/2+2)	3 to (e/2+5)

Notes:

- 1) Divide, Square Root, Remainder, and Modulus are implemented with an "early out" algorithm, where the iterative calculations are stopped if the current remainder becomes zero.
- 2) e = operand exponent difference
- 3) The pipeline is stalled 1 cycle for each denormal operand received
- 4) The pipeline is stalled 1 cycle when an underflow result is returned

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