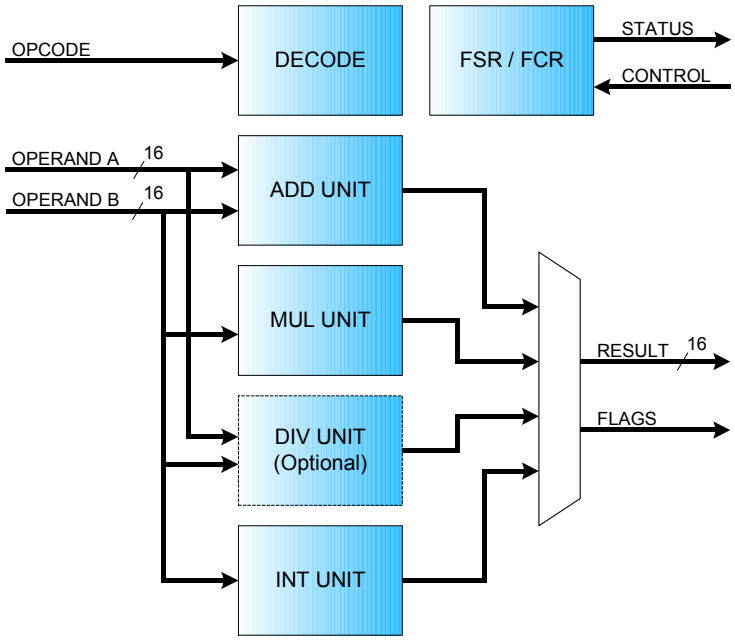
# FPHZ

## IEEE-754 Floating-Point Unit
## Half Precision with Flush-to-Zero Underflow




## Overview

The FPHZ is a co-processor unit providing floating-point computation compliant with the *ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic* (IEEE-754R Standard). It is designed to provide a powerful floating-point functionality for low-power, low frequency applications.

The FPHZ supports half precision operations in a 1-stage execution pipeline. The pipeline insures maximum performance in low-frequency applications, providing up to 200 MFLOPS on a 0.13u ASIC process. The host interface is clean and versatile, simplifying the interfacing to host processor pipelines.

## Features

- IEEE-754R compliant (except underflow)
- Flush-to-Zero underflow implementation
- Half precision instructions
- 1-stage execution pipeline
- Instructions provided
  - Add/Subtract/Absolute Difference
  - Multiply
  - Divide (optional)
  - Remainder/Modulus (optional)
  - Square root (optional)
  - Floating-Point Compare
  - Min/Max/Clip Functions
  - Floating-Point ↔ Integer Conversions
  - Round to Integer
  - Absolute Value/ Negate
  - Move
- Flag outputs support conditional branching or conditional execution
- All IEEE rounding mode supported
- All IEEE exception flags supported
- Masked and unmasked exception control
- Control and status registers

## IEEE-754R Compliance

The FPHZ is designed to provide a powerful floating-point capability while minimizing die size cost. To minimize unnecessary design size, some of the rarely used features of the IEEE specification are not implemented directly in the hardware design. The following IEEE-defined operations are not directly supported in FPHZ hardware, but can be supported with software support:

- Gradual Underflow
- Denormal Numbers

In place of gradual underflow, the FPHZ implements a flush-to-zero approach when underflow occurs. This feature allows the FPHZ to maintain a one-cycle throughput in all operand cases, and minimizes design size.

## Optional Divide Unit

The divide unit within the FPHZ design provides divide, square root, and remainder functions. In order to further minimize the design size, the FPHZ can be synthesized with or without a divide unit. Many multi-media applications can be implemented without the use of divide functions. For customers who need the absolute minimum area, this option is a must.

## Performance

Size: 14,000 NAND Gates, w/o divide unit
10,000 NAND Gates, w divide unit

Timing: 150 MHz on 0.18u
200 MHz on 0.13u

NOTE: The above performance data are estimates only, based on sample implementations using worst-case conditions. Achieved performance is highly dependent on the process technology, cell library, and synthesis tools used.

## Instruction Timing

| Instruction | Throughput / Latency |
|---|---|
| Add, Subtract, Difference, Multiply, Compare, Round to Integer | 1 |
| Single/Double Format Conversions Integer Conversions | 1 |
| Min, Max, Clip Functions | 1 |
| Absolute Value, Negate, Move | 1 |
| Divide | 1 to 7 |
| Square Root | 1 to 6 |
| Remainder, Modulus | 1 to (e/2+2) |

Notes:

1) Divide, Square Root, Remainder, and Modulus are implemented with an “early out” algorithm, where the iterative calculations are stopped if the current remainder becomes zero.
2) e = operand exponent difference



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